

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:  
a plurality of DRAM circuits;

a control circuit that receives a test control  
5 signal to perform a test control in which said  
plurality of RAM circuits are tested while the access  
to said plurality of DRAM circuits is subsequently  
changed for each row;

an input selector that is controlled by said  
10 control circuit and inputs a DRAM macro signal to said  
plurality of DRAM circuits at the time of a test; and

an output selector that is controlled by said  
control circuit, and outputs output signals of said  
15 plurality of DRAM circuits sequentially to a macro  
output terminal at the time of the test.

2. A semiconductor integrated circuit according  
to claim 1, wherein said control circuit is directly  
connected to a control signal input terminal to be  
controlled from said control signal input terminal and  
20 thereby the control circuit is directly controlled from  
said control signal input terminal.

3. A semiconductor integrated circuit according  
to claim 1, wherein said input selector that is  
controlled by said control circuit to input a DRAM  
25 macro signal to one of said plurality of DRAM circuits  
at the time of a normal operation.

4. A semiconductor integrated circuit according

Sub  
al

Sub  
a1

to claim 3, wherein said control circuit is directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuit is directly controlled from said control signal input terminal.

5

5. A semiconductor integrated circuit according to claim 1, wherein said output selector is controlled by said control circuit to output an output signal of one of said plurality of DRAM circuits to the macro output terminal at the time of a normal operation.

10

6. A semiconductor integrated circuit according to claim 5, wherein said control circuit is directly connected to said control signal input terminal to be directly controlled from said control signal input terminal and thereby is controlled directly from said control signal input terminal.

15

7. A semiconductor integrated circuit according to claim 1, wherein said control circuit performs a test control of said plurality of DRAM circuits in such a manner that the access to first rows of said plurality of DRAM circuits is performed while successively changing the access to said plurality of DRAM circuits, and, following the access to the first rows of said plurality of DRAM circuits, the same access as that to the first rows of said plurality of DRAM circuits is performed from the next rows to the last rows of said plurality of DRAM circuits while

20

25

TOP SECRET

**Abstract**

10

15

20

25

11. A semiconductor integrated circuit according to claim 9, further comprising an input selector for

Sub  
a1

receiving a DRAM macro signal.

12. A semiconductor integrated circuit according to claim 11, wherein said control circuits are directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuits are directly controlled from said control signal input terminal.

13. A semiconductor integrated circuit according to claim 9, wherein said output selector is controlled by said control circuit to output an output signal of one of said plurality of DRAM circuits to the macro output terminal at the time of a normal operation.

14. A semiconductor integrated circuit according to claim 13, wherein said control circuits are directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuits are directly controlled from said control signal input terminal.

15. A semiconductor integrated circuit according to claim 9, wherein said control circuits performs a test control of said plurality of DRAM circuits in such a manner that the access to first rows of said plurality of DRAM circuits is performed while successively changing the access to said plurality of DRAM circuits, and, following the access to the first rows of said plurality of DRAM circuits, the same access as that to the first rows of said plurality of

Sub  
a/

DRAM circuits is performed from the next rows to the last rows of said plurality of DRAM circuits while successively changing the access to said plurality of DRAM circuits for each row.

5           16. A semiconductor integrated circuit according to claim 15, wherein said control circuits are directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuits are directly controlled from said control signal input terminal.

10           17. A semiconductor circuit comprises:

          a plurality of DRAM circuits;

          a control circuit that receives a control signal and controls said plurality of DRAM circuits simultaneously and independently from each other;

15           an input selector for supplying a DRAM macro signal input to one of said plurality of DRAM circuits;

          an output selector that selects an output signal of one of said plurality of DRAM circuits and outputs the output signal to a macro output terminal.

20           18. A semiconductor integrated circuit according to claim 17, wherein on receiving the control signal, said control circuit controls said plurality of DRAM circuits so that data is read from said plurality of DRAM circuits sequentially and transferred to the outside of the DRAM circuits.

25           19. A semiconductor integrated circuit according

[illegible]